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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,449	12/10/2001	Robert Thomas Bailis	RPS920010127US1	5286

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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/016,449	BAILIS ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 12-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 12-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 and 12-19 have been examined. Claims 1-15 were pending. Claims 6, 9 and 13 have been amended. Claims 10 and 11 have been canceled. Claims 16-19 are newly submitted.

2. The Examiner would like to point out to the Applicants that newly submitted claims 17-19 were not mentioned in the remarks.

Response to Arguments

3. Applicant's arguments with respect to claims 1-9 and 12-19 have been considered but are moot in view of the new ground(s) of rejection.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1 and 16 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/016448. Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant application recites, among other identical limitations, *a field programmable gate array (FPGA) function coupled to the at least one bus and the plurality of internal signals, the FPGA function including a debug client function that observes and manipulates the at least one bus and the plurality of internal signals*. Claim 1 of copending Application No. 10/016448 recites *a field programmable (FP) function coupled to the at least one bus and at least a portion of the plurality of internal signals, wherein the FP function provides access to internal signals for observation and control without requiring input/output (1/0) pins to access the internal signals*.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-9 and 12-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Shen et al. (US-6829751), hereinafter Shen.

Claim 1:

Shen teaches a standard cell, the standard cell (Fig. 2, circuit 102) including a plurality of logic functions (Fig. 2, circuit 110, 112, 114); at least one bus coupled to at least a portion of the logic functions; a plurality of internal signals from the plurality of logic functions (Fig. 2, bus and internal signals 140, 142, 144, 146); and a field programmable gate array (FPGA) function (Fig. 2, FPGA Core) coupled to the at least one bus (Fig. 2, bus 140, 142, 144, 146, 152) and the plurality of internal signals, the FPGA function including a debug client function that observes and manipulates (Col. 2. ll. 39-44, col. 4, ll. 22-24, col. 5, ll. 1-4, col. 6, ll. 21-25, 45-56) the at least one bus and the plurality of internal signals. (Col. 2, l. 39 to col. 6, l. 65).

Claim 16:

Shen teaches a standard cell (Fig. 2, circuit 102) including a plurality of functional units, each functional unit having an internal signal (Fig. 2, circuit 110, 112, 114); a bus

coupled to at least a portion of the plurality of functional units; a field programmable gate array (FPGA) (Fig. 2, FPGA Core) coupled to the bus (Fig. 2, 152) and the plurality of functional units, the FPGA including a debug client operable to directly observe and manipulate the bus and the internal signal of each of the functional units (Col. 2. ll. 39-44, col. 4, ll. 22-24, col. 5, ll. 1-4, col. 6, ll. 21-25, 45-56), where each internal signal being directly observed and manipulated is external to the FPGA (Fig. 2).

Claims 2, 10 and 17:

Shen teaches at least one bus comprises an internal bus (Fig. 2, buses 140, 142, 144, 146).

Claims 3 and 11:

Shen teaches the debug client function (FPGA Core 116) observes and manipulates at least one point of interest on the standard cell. (Col. 5, ll. 1-4, col. 6, ll. 45-56).

Claims 4, 12 and 19:

Shen teaches debug client function (FPGA Core 116) is programmed by a server (Debugging Workstation 104). (Col. 3, ll. 49-54).

Claim 5:

Shen teaches "the debug client function (FPGA core 116) further includes an external communicator logic function for receiving and transmitting information to a server (Debugging Workstation 104)" (Col. 3, ll. 25-26, col. 5, ll. 13-20), and "selector logic coupled to the at least one bus and the plurality of internal signals" (Col. 6, ll. 49-52). Shen also teaches "an interface logic coupled between the external communicator

logic and the selector logic for providing communication therebetween" in that there is circuitry within the FPGA core 116 programmed by the Debugging Workstation 104 (Col. 5, 13-25) to execute debugging diagnostics, some of which are outlined in col. 6, ll. 1-57).

Claims 6 and 13:

Shen teaches that the interface logic comprises of a storage logic function for storing a state of signals of interest from the selector logic and providing the state to a server (on chip registers, col. 5, ll. 36-39), a comparator logic function coupled to the storage logic function for comparing the signals of interest from the selector block function (Col. 5, ll. 39-45, col. 6, ll. 32-44), and an output logic function coupled to the comparator logic function for controlling the internal signals on the ASIC (Col. 3, ll. 22-27, ll. 49-54).

Claims 7 and 14:

Shen teaches the server utilizes the debug client to debug hardware within at least one of the plurality of logic functions. (Col. 2, ll. 42-45, Fig. 2).

Claims 8, 15 and 18:

Shen teaches the server utilizes the debug client to debug software within at least one of the plurality of logic functions. (Col. 6, ll. 1-63).

Claim 9:

Shen teaches a debug client function within an application specific integrated circuit (ASIC, the debug client function being within a field programmable gate array (FPGA) function as per the rejection of claim 1. Shen also teaches the client debug

function comprises an external communicator logic function for receiving and transmitting information concerning a plurality of internal signals of the ASIC to a server, selector logic coupled to the at least one bus of the ASIC and the plurality of internal signals, and an interface logic coupled between the external communicator logic and the selector logic for providing communication therebetween in the rejection as per the rejection of claim 5. Shen further teaches the at least one bus comprises and internal bus, and the debug client function observes and manipulates at least one of the plurality of internal signals of the ASIC as per the rejection of claim 1.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

10/18/05

GUY LAMARRE
PRIMARY EXAMINER